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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,973	04/05/2001	Norio Hirashita	OKI.227	3710

7590 09/25/2003

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EXAMINER

MALDONADO, JULIO J

ART UNIT PAPER NUMBER

2823

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,973	HIRASHITA ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 July 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-16 and 23-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-16 and 23-30 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. Applicant's cancellation to claims 17-22 is acknowledged. Claims 23-30 are newly added. Thus, claims 1-16 and 23-30 are pending in this application.

Response to Arguments

2. Applicant's arguments, see pages 16-17, filed 07/12/2003, with respect to the rejection(s) of claim(s) 1-1-16 under USC 35 §112 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Imai (U.S. 6,344,675 B1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3, 5, 7, 9, 11, 13, 15 and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (U.S. 6,344,675 B1).

Imai (Figs.12-13D) teach a low resistance SOI-FET device including an insulating layer (2); a semiconductor layer (3) formed on the insulating layer (2), wherein the semiconductor layer (3) includes the channel region therein; a pair of impurity layers (9, 10) formed in regions which are respectively in contact with the channel region in the source region and the drain region; and a pair of metallic silicide layers (16) respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers (16) are respectively in contact with the pair of impurity layers (9, 10), wherein

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bottom surfaces of the pair of metallic silicide layers (16) extend to bottom surfaces of the semiconductor layer (3), wherein the thickness of the metallic silicide layers (16) is equal to or more than 80% of form an upper surface of the metallic silicide layers (16) to the bottom surface of the semiconductor layer; wherein the metallic silicide layers (16) are composed of refractory metal and silicon, and wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, wherein the metallic silicide layer comprises cobalt silicide (column 22, line 66 – column 25 line 21 and column 43, line 6 – column 48, line 63).

Imai fails to expressly teach that the ratio of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X_0 to Y_0 , and X , Y , X_0 and Y_0 satisfy the following inequality: $(X/Y) > (X_0/Y_0)$; wherein a ratio of cobalt to silicon is one to α ($1 < \alpha < 2$); and wherein a contact specific resistance between the metallic silicide layers and the impurity layers is less than $1 \times 10^{-7} \Omega\text{-cm}^2$. However, the selection of the claimed stoichiometric ratio and specific resistance is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above-mentioned stoichiometric ratio and resistance to arrive at the claimed invention.

5. Claims 2, 4, 6, 8, 10, 12, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai ('675 B1) as applied to claims 1, 3, 5, 7, 9, 11, 13 and 15 above, and further in view of the Applicants Admitted Prior Art.

Imai substantially teaches all aspects of the invention but fails to show wherein said FET device includes a depletion layer, which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof. However, the prior art teaches FET devices include a depletion layer, which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof (Instant pages 1 – 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imai and the prior art to enable including the depletion layer of the prior art in the device of Imai.

6. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is (703) 305-3432. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at (703) 306-0098 and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone

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are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at (703) 308-0956.

flm
JMR
9/21/03

G. Fourson
George Fourson
Primary Examiner